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Modeling of a Stacked Power Module for Parasitic Inductance Extraction

by Steven Kaplan

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14. ABSTRACT
Power switching modules inevitably suffer from compromised electrical performance due to limitations imposed by standard planar packaging arising from issues of heat dissipation, reliability, and parasitic inductance. An improved packaging approach has been proposed to simultaneously address each of these issues, including parasitic inductance. Parasitic inductance has a particularly detrimental effect on metal–oxide–semiconductor field-effect transistor switching characteristics due to signal overshoot. This approach makes use of multifunctional components as concurrent electrical, thermal, and mechanical attachments. The power devices in the resulting module design are stacked between copper layers with an integrated heat sink. By stacking devices, the module's parasitic inductance should be reduced, with concurrent improvement of reliability and heat dissipation, in comparison to traditional planar packaging. This report describes modeling used to extract the predicted parasitic inductance of a stacked half-bridge switching module, by performing magnetic-field simulations to derive frequency-dependent impedances.

15. SUBJECT TERMS
power module, half-bridge, stacked devices, overshoot, parasitic inductance, multifunctional components

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1. Introduction

Parasitic impedances are critical to the achievable performance of power electronics components, and especially so for those used in switching applications. Wide bandgap semiconductor devices, in general, and silicon carbide (SiC) devices, in particular, are used in fast switching applications, which seek to take advantage of their exceptional performance capabilities. However, these capabilities are limited by the parasitic inductance of the packages in which the SiC devices are contained. High-speed and/or high-frequency applications pose a potent challenge to maintaining switching performance due to the resulting large oscillation ringing and overshoot in the switching waveforms attributable to parasitic inductances in the device package and its external circuit.[1] Power electronics switching voltages are typically de-rated by 50% to safely accommodate anticipated over-voltage due to various phenomena related to device fabrication and packaging. Primary among these phenomena is voltage overshoot due to parasitic inductance, particularly in high current, fast switching applications. Since the overshoot voltage is directly proportional to parasitic inductance, minimizing the module package inductance should allow for less de-rating of the switching voltage for a given switching current and speed.

2. The Stacked Power Module

A typical power module layout is shown in Fig. 1 with a cross-sectional view of its various components. Note that this design employs single-function components spread out over the entire package region to address the electrical, thermal, and mechanical requirements of the module. The power module being modeled in this work consists of a half-bridge configuration with a stacked die and integrated cooling. The stacked elements of the module simultaneously provide thermal and electrical contact. These multifunctional components (MFCs) compose the constituent sections that make up the power module. The module is shown in Fig. 2 next to a half-bridge circuit schematic. The half-bridge design is being considered because it is the foundation of many power circuits (inverters and converters). The power module, as described, is both modular and scalable to accommodate any number of configurations of diodes and switching devices.[2] This particular half-bridge module consists of 2 diodes and 2 switches, such as insulated gate bipolar transistors (IGBTs) or metal–oxide–semiconductor field-effect transistors (MOSFETS). The stacked arrangement of the MFCs reduces the lengths and number of constrictive electrical paths, especially wire-bonds. The switches are packaged in series rather than the more typical antiparallel configuration, to further reduce inductance.[3]

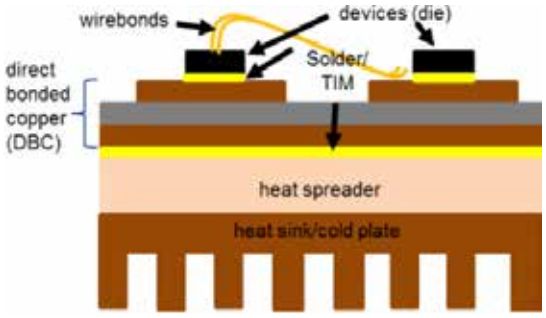

Fig. 1 Standard power module configuration

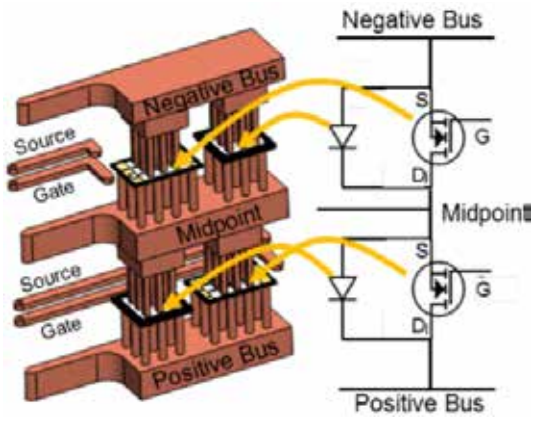

Fig. 2 Half-bridge circuit schematic indicating the location of the 2 switches and 2 diodes in the assembly

The electrically conductive layers for the power module are fabricated from copper, while all the devices are primarily SiC. The base layer acts as the positive bus in the circuit. It connects the drain of the switching device to the cathode of the associated diode. The middle layer consists of a conductor that acts as the midpoint on the circuit schematic. It electrically connects the source of the lower switching device and the anode of the lower diode to the cathode of the upper diode and the drain of the upper switching device. The top layer shown in Fig. 2 acts as the negative bus in the half-bridge module connecting the source of the upper switching device to the anode of the diode.

3. Magnetic-Field Simulation Model

The model developed to extract the inductance of the stacked power module was created in COMSOL Multiphysics Simulation Software. Within the AC/DC module of COMSOL, a magnetic-field physics simulation was performed. This simulation uses a current driven “lumped port” defined between the negative bus and the midpoint terminals of the stacked module. The study analysis for the

simulation was done in the frequency domain from 100 kHz to 100 MHz. This frequency range encompasses the relevant wide bandgap signal spectrum corresponding to the switching applications anticipated for this power module. Inductive impedance characteristics of the power module are negligible at frequencies below 100 kHz. This is because the self-resonance frequency of the power module, where the impedance transitions from capacitive to inductive, is well above 1 MHz, which is apparent from the results presented in the subsequent sections of this report.

The COMSOL model geometry for the stacked power module is shown in Fig. 3. The purple regions represent the copper components that form the bulk of the module. The SiC MOSFETs and diodes are rendered as clear with black framing of their boundary regions. The 4 aluminum wire-bond connections from the source and gate lines are rendered as straight black segments. The acrylic module case, including cooling fluid ports, is outlined in gray. The module components are immersed in NOVEC 7500 engineering fluid, which resides within the outer case. The various properties of this fluid, such as dielectric permittivity and resistivity, were manually defined in the COMSOL model. The lumped port, through which the power module is excited in the model analysis, is indicated by the narrow rectangular prism (outlined in gray) extending between the negative bus and the midpoint.

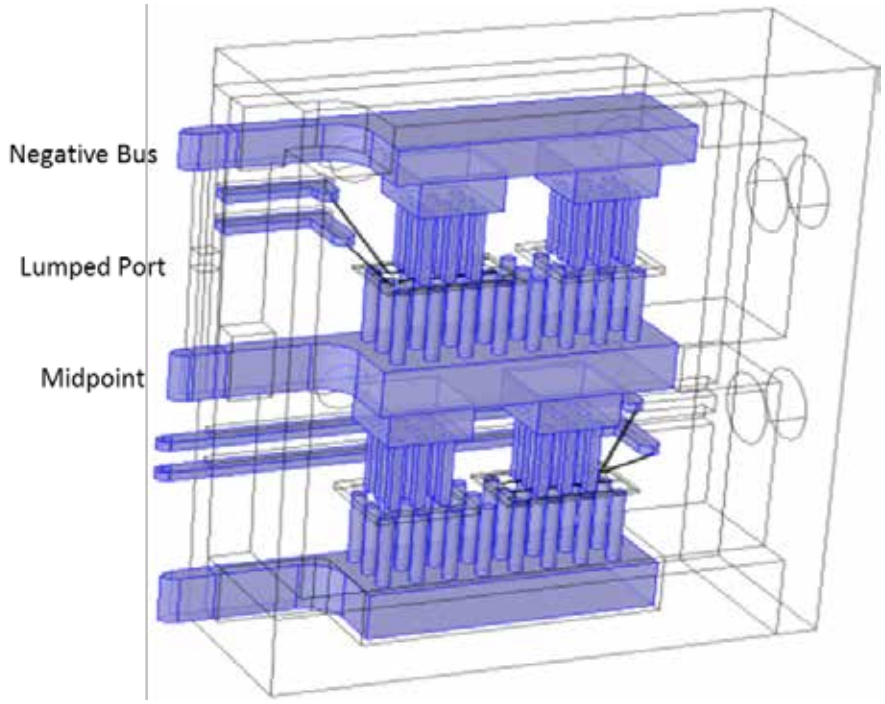

Fig. 3 Half-bridge simulation model schematic

The circuit diagram corresponding to the model of the half-bridge power module is shown in Fig. 4. The magnetic-field analysis in the model is performed on the section of Fig. 4 enclosed in red. Note that the negative bus corresponds to D_1, the midpoint to S_1D_2, and the positive bus to S_2. Therefore, the diagram in Fig. 4 is inverted relative to the representation in Fig. 3.

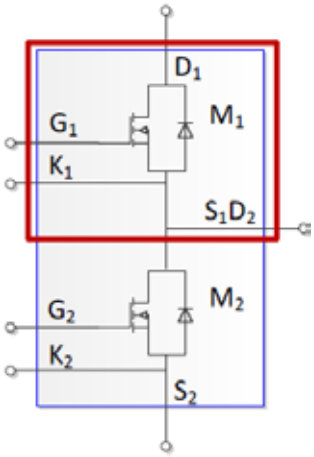

Fig. 4 Modeled half-bridge circuit, with the section containing the excitation port (D_1-S_1D_2) enclosed in red

4. Modeling Results

The impedances derived from the model at the lumped port of the stacked power module are tabulated in Table 1. Notice that the imaginary impedance component (i.e., reactance) transitions from negative to positive between 2 and 10 MHz. Frequency-domain impedance analysis at the excitation terminals leads to a series resonant impedance plot with minimum magnitude at the self-resonant frequency (SRF).[4] The transition of the port reactance from negative (capacitive) to positive (inductive) in the power module is also located within this spectral region. Above this transition frequency, the module parasitics are primarily inductive and can be extracted from the reactance values.

Table 1 Impedance of power module for each frequency in model analysis

Frequency (MHz)	Lumped port impedance (Ω)
0.1000	0.024147 – 0.033403i
1.000	0.24147 – 0.33403i
2.000	0.48295 – 0.66805i
10.00	0.56212 + 0.24714i
50.00	2.8106 + 1.2357i
100.0	1.5599 + 6.0842i

The transition from capacitive to inductive reactance is well illustrated by the frequency plot in Fig. 5. The capacitive reactances become more negative as frequency rises, until there is a transition to positive reactance between 2 and 10 MHz. Thereafter, the reactances rise with frequency from 10 to 100 MHz. The minimum impedance magnitude at the SRF is consistent with this frequency response pattern, as shown in Fig. 6.

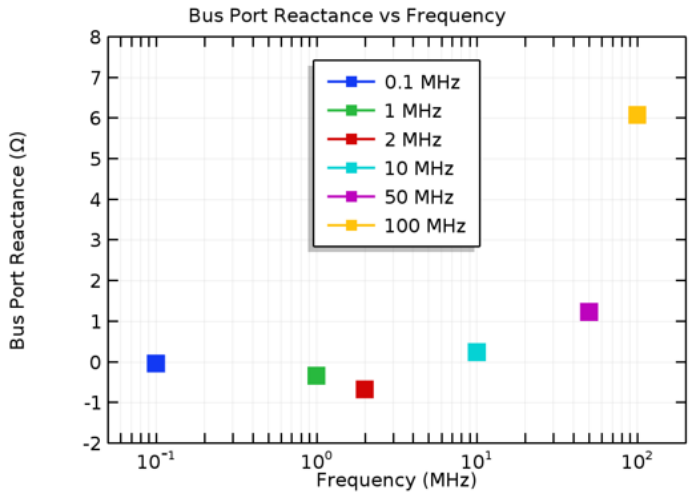

Fig. 5 Frequency plot of half-bridge reactance

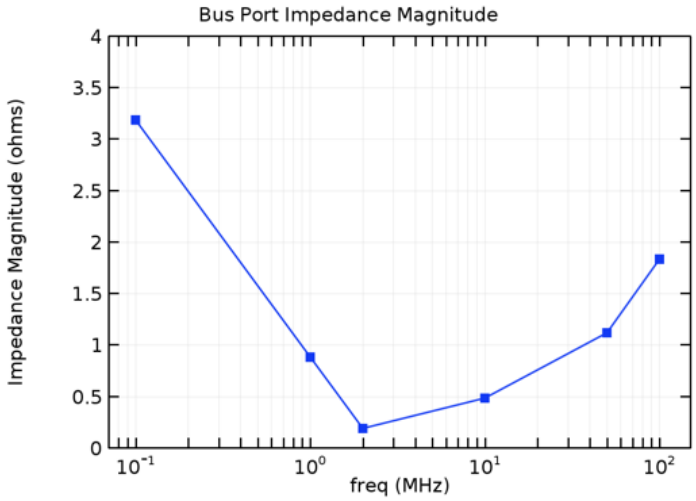

Fig. 6 Frequency plot of impedance magnitude

Based on the reactance transition to inductive values between 2 and 10 MHz, the inductance for the half-bridge was extracted from the reactance values at 10, 50, and 100 MHz. Each inductance value can be found by dividing the corresponding reactance by 2pw. These inductances are plotted, along with the reactance values, in Fig. 7. The reactance rises linearly from 2 to 50 MHz, and this linearity persists

at simulation frequencies to at least 60 MHz. However, the impedance and reactance rise more rapidly as the frequency approaches 100 MHz. Based on consultations with COMSOL technical support personnel, it is believed that this nonlinear behavior at the higher frequencies may be due to device subdomains that were defined in the computer-aided design software model, which was imported into the COMSOL platform for the physics analysis. The boundary traces of these subdomains are visible in Fig. 3. They create meshing issues that may cause instabilities in the model analysis at higher frequencies. These meshing issues were successfully dealt with, for the most part, but may be affecting the high-frequency solutions near 100 MHz. As such, the subdomain boundaries will be removed and the analysis revisited in subsequent modeling. This will be part of a continuing device package optimization effort, which will include extensive empirical comparisons.

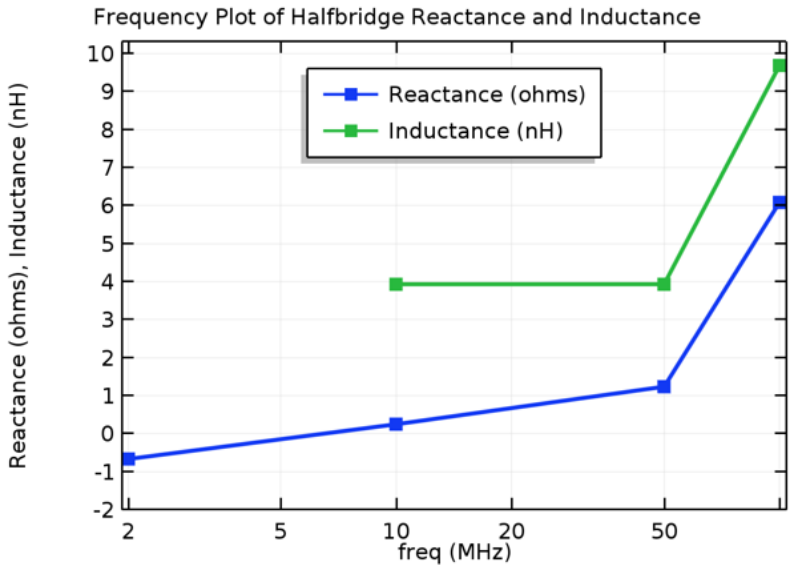

Fig. 7 Comparison of the modeled reactance and inductance

The parasitic inductance extraction results of the modeling analysis are summarized in Table 2. As noted, there is remarkable consistency in the inductance values derived from the modeled impedance of the stacked power module. The predicted inductance is calculated to be 3.93 nH for all excitation frequencies in the model beyond the resonance transition, except at the maximum study frequency of 100 MHz, where it rises to 9.68 nH. However, even without attributing this increase to meshing anomalies at the device subdomain boundaries, the modeling results indicate that the stacked half-bridge power module design has significantly lower parasitic inductances than those of traditional planar configurations, which are typically an order of magnitude higher (near or above 50 nH).[3]

Table 2 Parasitic inductance values extracted at frequencies above self-resonance

Frequency (MHz)	Reactance (Ω)	Inductance (nH)
10	0.247	3.93
20	0.494	3.93
30	0.741	3.93
50	1.236	3.93
60	1.483	3.93
100	6.084	9.68

5. Conclusions and Future Work

Preliminary modeling of the impedance characteristics of a stacked half-bridge power module was performed to investigate its efficacy in limiting parasitic inductance. This stacked design makes use of compact MFCs to address cooling, reliability, and reduction of parasitics. Magnetic-field modeling reveals that the parasitic inductance of this design is significantly lower than is generally found in standard planar module configurations. The inductance values predicted by the model ranged from about 4 to 10 nH, well below the usual parasitic inductance typically seen by power modules of the planar type, which are on the order of 50 nH or higher. This reduction in inductance is likely due to more compact electrical connections and elimination/shortening of package wire-bonds. Follow-on modeling will be performed in the future, as part of a co-engineering/co-design effort, and will incorporate empirical data and comparisons with different power module designs.

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List of Symbols, Abbreviations, and Acronyms

AC	alternating current
ARL	US Army Research Laboratory
DC	direct current
IGBT	insulated gate bipolar transistor
MFC	multifunctional component
MOSFET	metal–oxide–semiconductor field-effect transistor
SiC	silicon carbide
SRF	self-resonant frequency

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